ABSTRACT

A DRAM adopting a single-intersection memory cell array having randomly accessible data registers accessed whenever the chip is accessed externally. When data items recorded in the data registers are simultaneously written in the memory cell array, the data items are encoded. When data items are read from the memory cell array into the data registers, the data items are decoded. The margin is enhanced because array noise derived from reading is reduced. In addition, the access time of the DRAM is also reduced.